Announcements

- Homework 7 due Friday in class.
- Design project posted: LED driver with XOR input.
- Office hours today W 2-3pm, Th 1-2pm in EE218.

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Dynamic Power Dissipation

- Each cycle, the load C is charged (from V_{DD}) and discharged (to ground).
- Thus, the energy dissipated per cycle is:

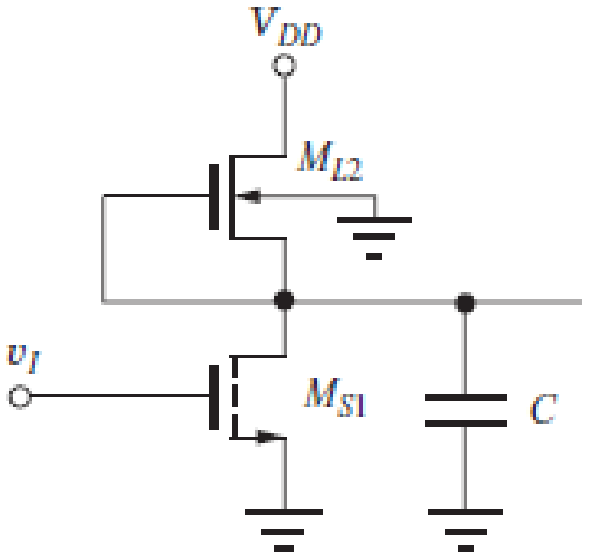
$$E_D = V_{DD}\int_0^\infty i(t)dt \cong V_{DD}\int_0^\infty C\frac{dv_c}{dt}dt$$

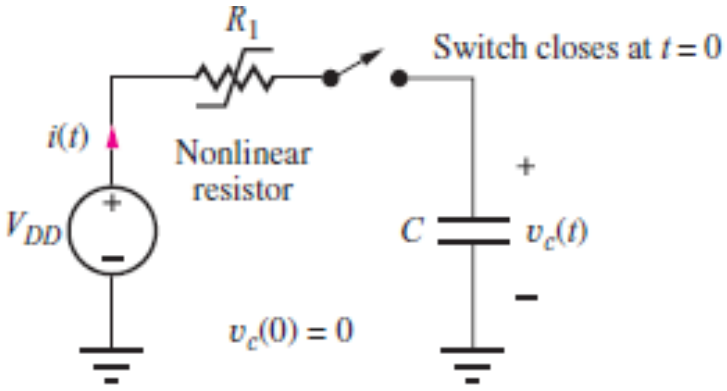
$$= V_{DD}C\Delta v \cong CV_{DD}{}^2$$

- Dynamic power dissipation is:

$$P_D = E_D f = C\Delta v V_{DD} f \cong CV_{DD}{}^2 f$$

- Energy stored in C is $CV_{DD}{}^2/2$, so half the energy is dissipated each half-cycle





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Inverter Comparison

- To get same V_L, same load current when v_o=V_L.
- For fast switching (and best VTC), want maximum pull-up (load) current.
  - PMOS > Depletion > R > Linear > Saturation
  - Body effect degrades Depl, Lin, Sat

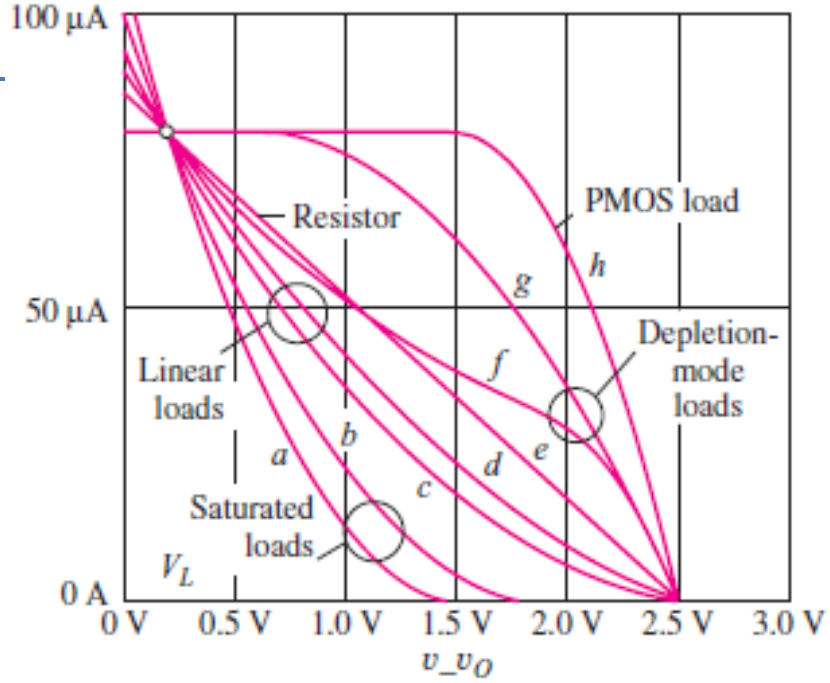

Figure 6.47 A comparison of NMOS inverter load device characteristics with current normalized to 80 µA for $v_o = V_L = 0.20$ V. (a) Saturated load including body effect, (b) saturated load without body effect, (c) linear load with body effect, (d) linear load without body effect, (e) 28.8-kΩ load resistor, (f) depletion-mode load with body effect, (g) depletion-mode load with no body effect, (h) PMOS load transistor for the pseudo NMOS inverter.

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PMOS Logic

- PMOS logic is just like NMOS logic, except polarities are reversed.
- Could replace (-2.5V, 0V) with (0V, 2.5V), B at 2.5 V.

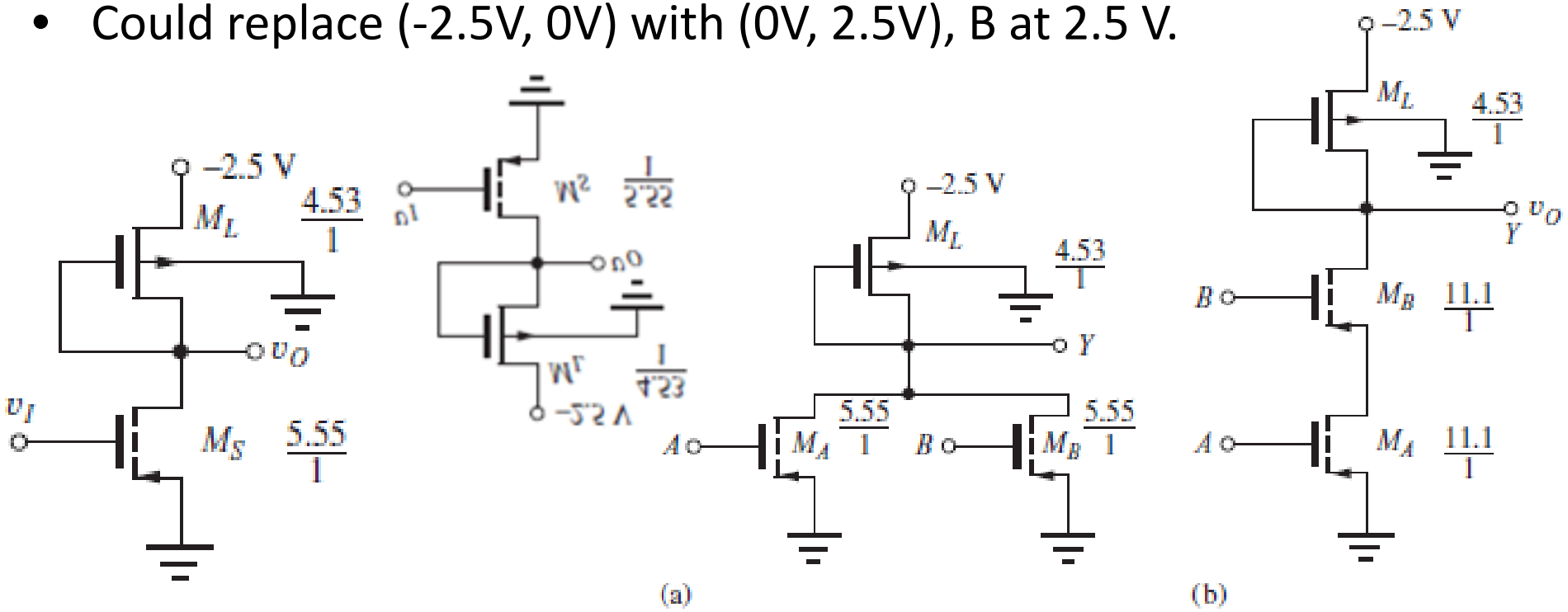

Figure 6.50 Two-input PMOS gates: (a) NOR gate and (b) NAND gate.

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EE 331 Devices and Circuits I

Chapter 7

CMOS Logic Design

CMOS Technology

- NMOS microprocessors dissipates too much static power
- CMOS solves the power dissipation problem and dominates digital IC design today
- CMOS: Complementary MOS
  - Needs both PMOS and NMOS transistors to be built in the substrate
  - Increase of process complexity, more area, higher cost

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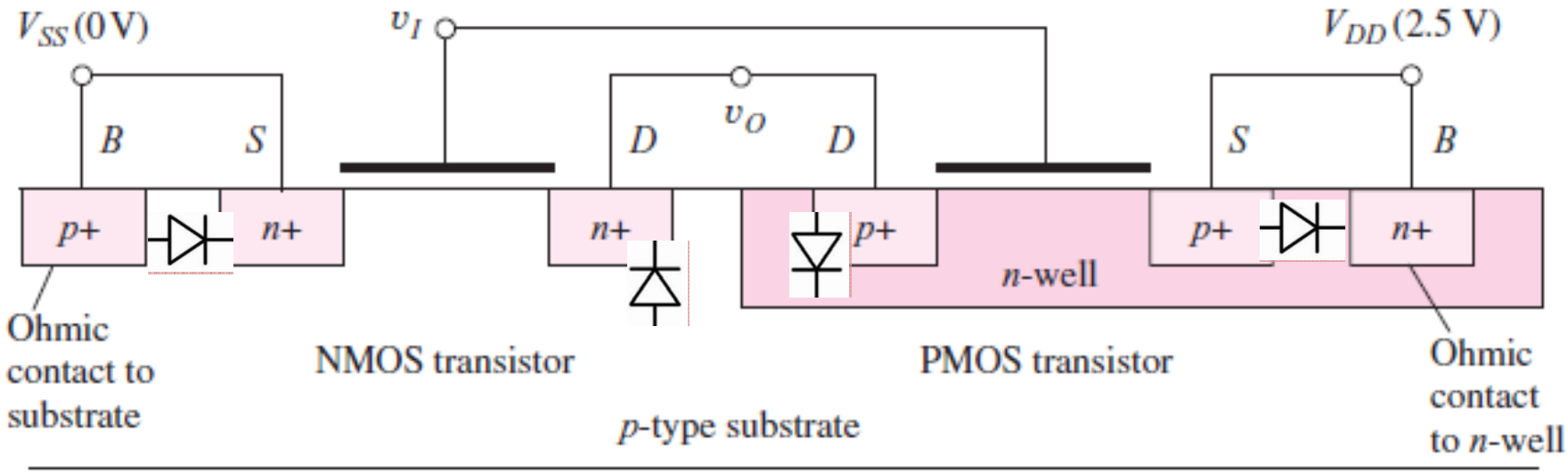
CMOS Technology

- PMOS and NMOS fabricated on the same wafer
- “n-well” implantation needed
- Diode between N/P MOS body terminals reverse biased



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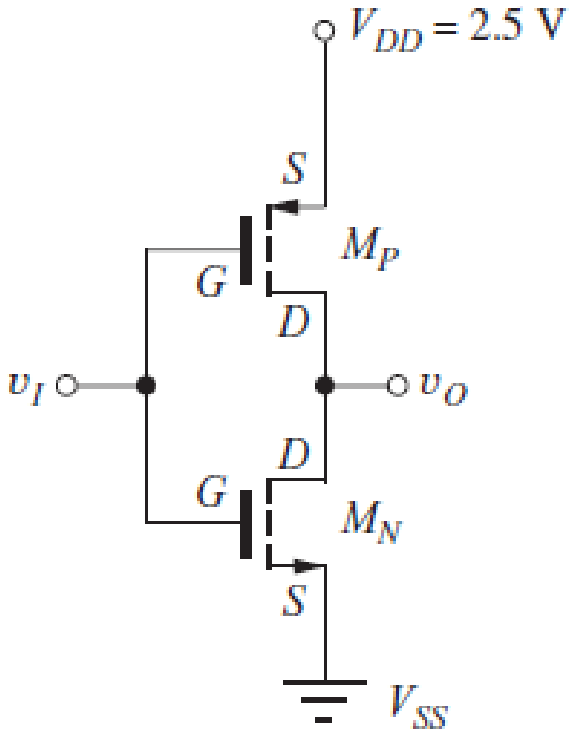
CMOS Connections

- V_{DD} connected to Source of PMOS
- V_{SS} connected to Source of NMOS
- Both gates are connected to input
- Both drains are connected as output
- Bodies are connected to their respective sources
  - No body effect!



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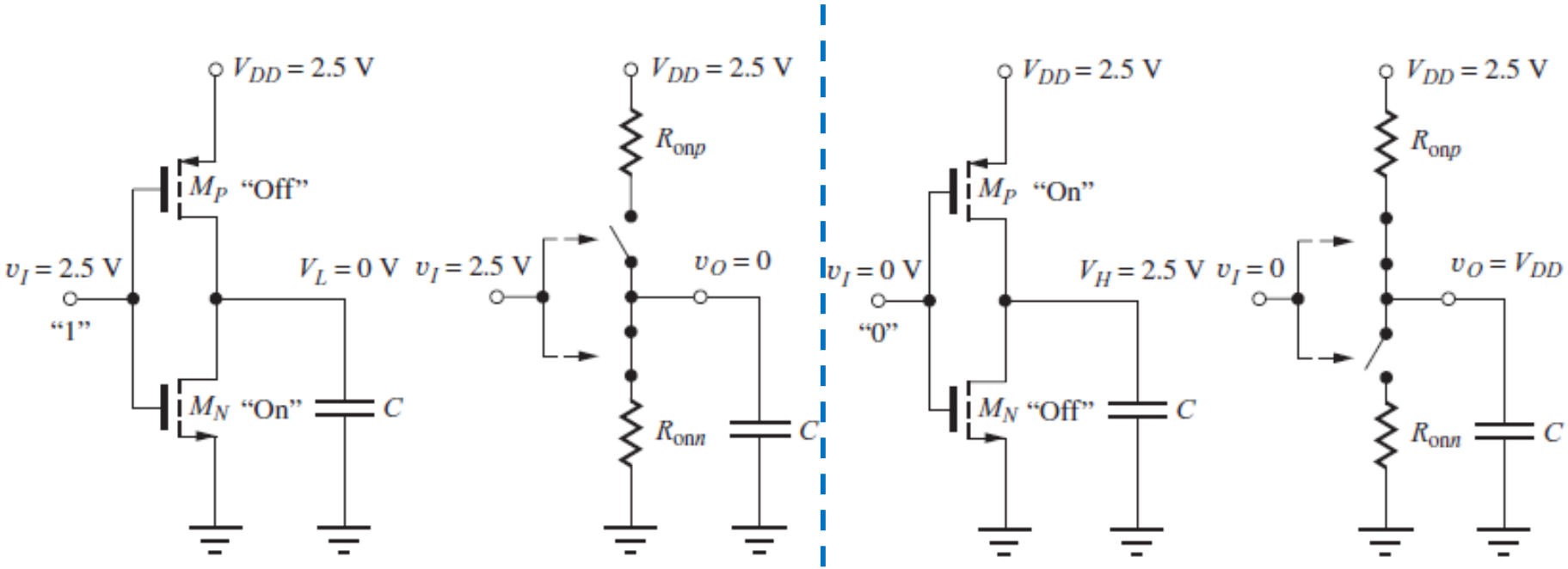
CMOS Inverter static behavior



v_I High, v_O Low

v_I Low, v_O High

- $v_I = V_{DD}$ (High), M_N on, M_P off, $v_O = 0$ (Low)
- $v_I = 0$ (Low), M_N off, M_P on, $v_O = V_{DD}$ (High)
- $i_D = 0$ for both cases: No static power dissipation!

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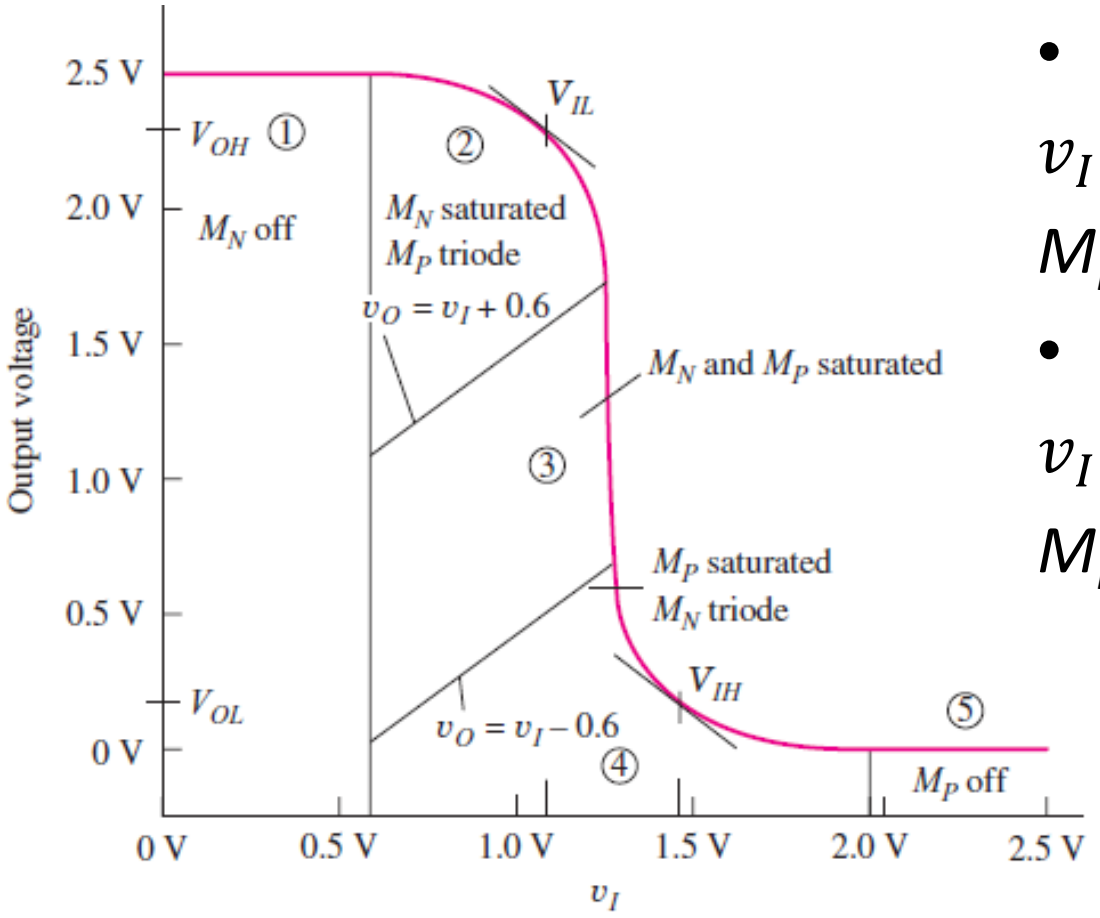
CMOS Voltage Transfer Characteristics



Symmetrical CMOS Inverter ($K_p = K_n$)

- Region 1:

$v_I < V_{TN} = 0.6$ V,

M_N off, $v_O = 2.5$ V

- Region 5:

$v_I > V_{DD} + V_{TP} = 1.9$ V,

M_P off, $v_O = 0$ V

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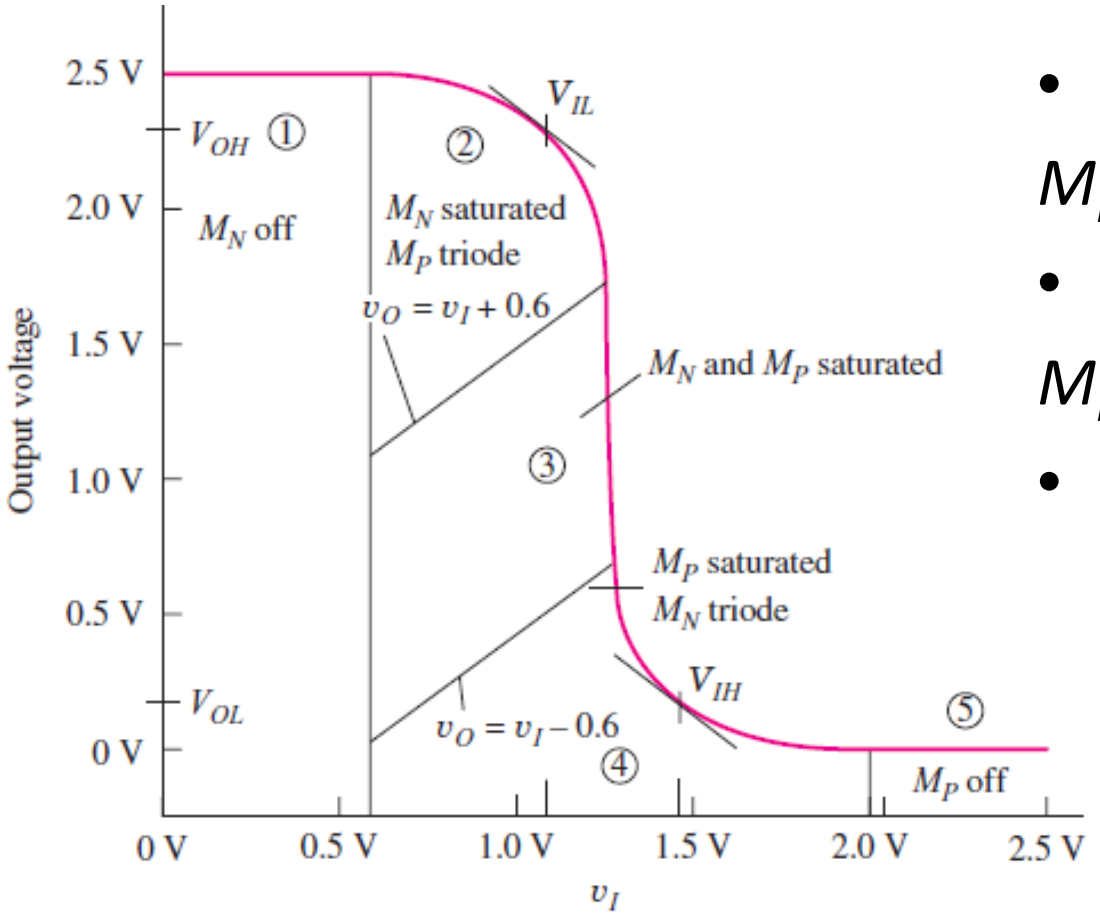
CMOS Voltage Transfer Characteristics



Symmetrical CMOS Inverter ($K_p = K_n$)

- Region 2:

M_N saturated, M_P triode

- Region 3:

M_N saturated, M_P saturated

- Boundary between 2-3:

$$v_{DSP} = v_{GSP} - V_{TP} \Rightarrow$$
$$v_O = v_I + 0.6$$

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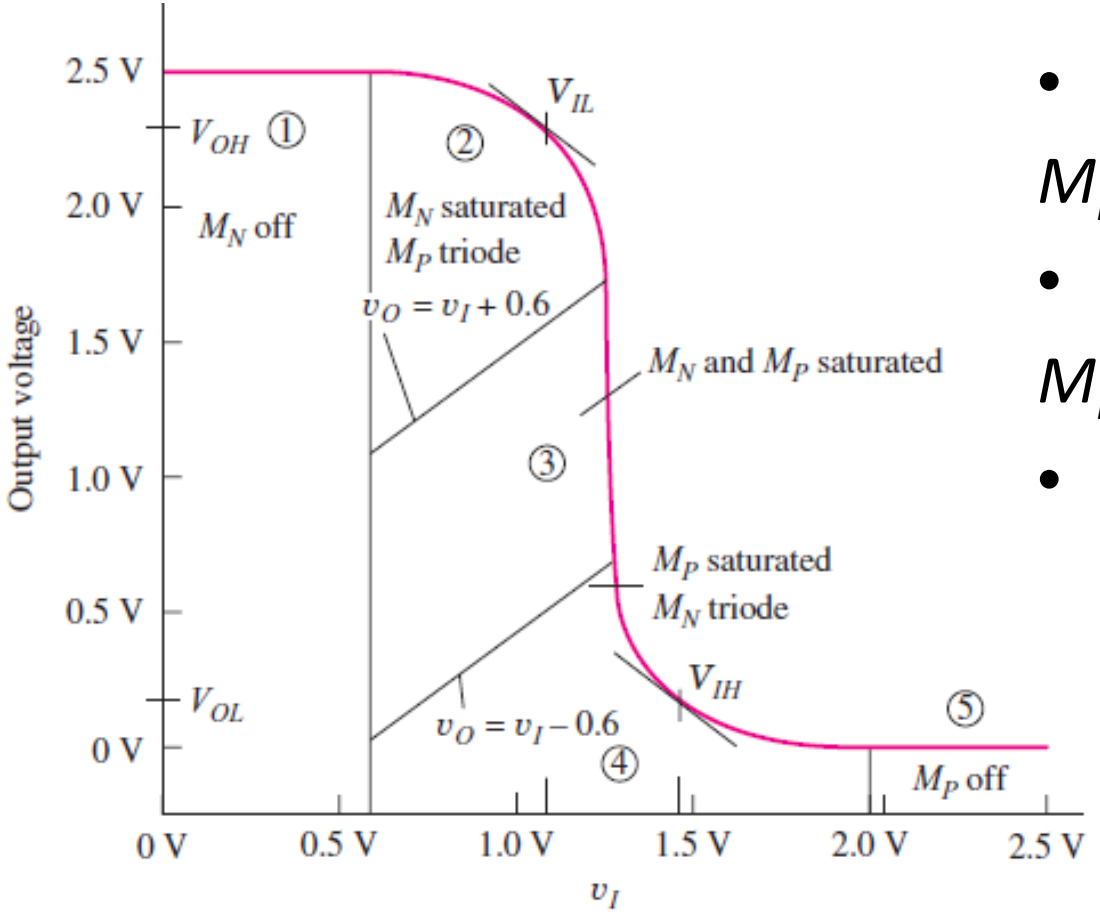
CMOS Voltage Transfer Characteristics



Symmetrical CMOS Inverter ($K_p = K_n$)

- Region 4:

M_P saturated, M_N triode

- Region 3:

M_P saturated, M_N saturated

- Boundary between 3-4:

$$v_{DSN} = v_{GSN} - V_{TN} \Rightarrow$$
$$v_O = v_I - 0.6$$

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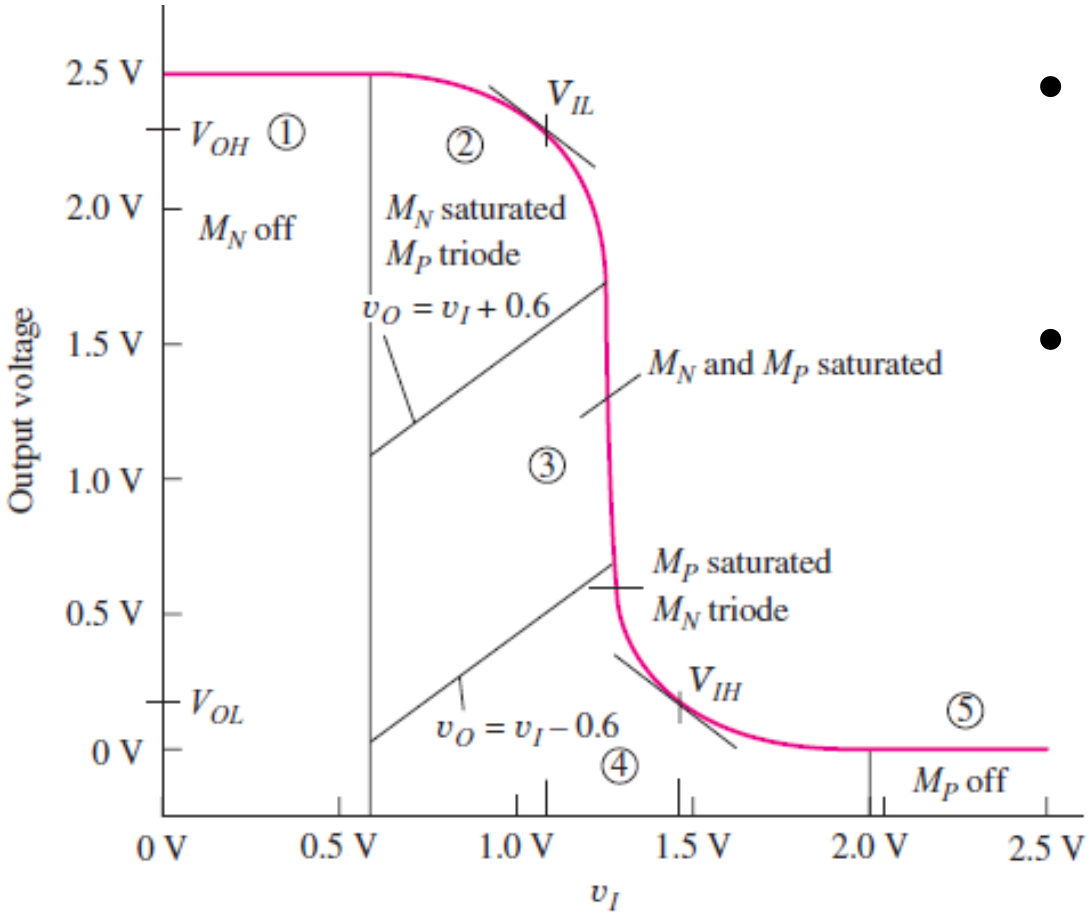
CMOS Voltage Transfer Characteristics



Symmetrical CMOS Inverter ($K_p = K_n$)

- For CMOS
  - $V_H = V_{DD}$, $V_L = 0$.
  - $\Delta V = V_H - V_L = V_{DD}$
- For symmetrical design ($K_p = K_n$):
  - Transition between V_H and V_L centered at $V_I = V_{DD}/2$

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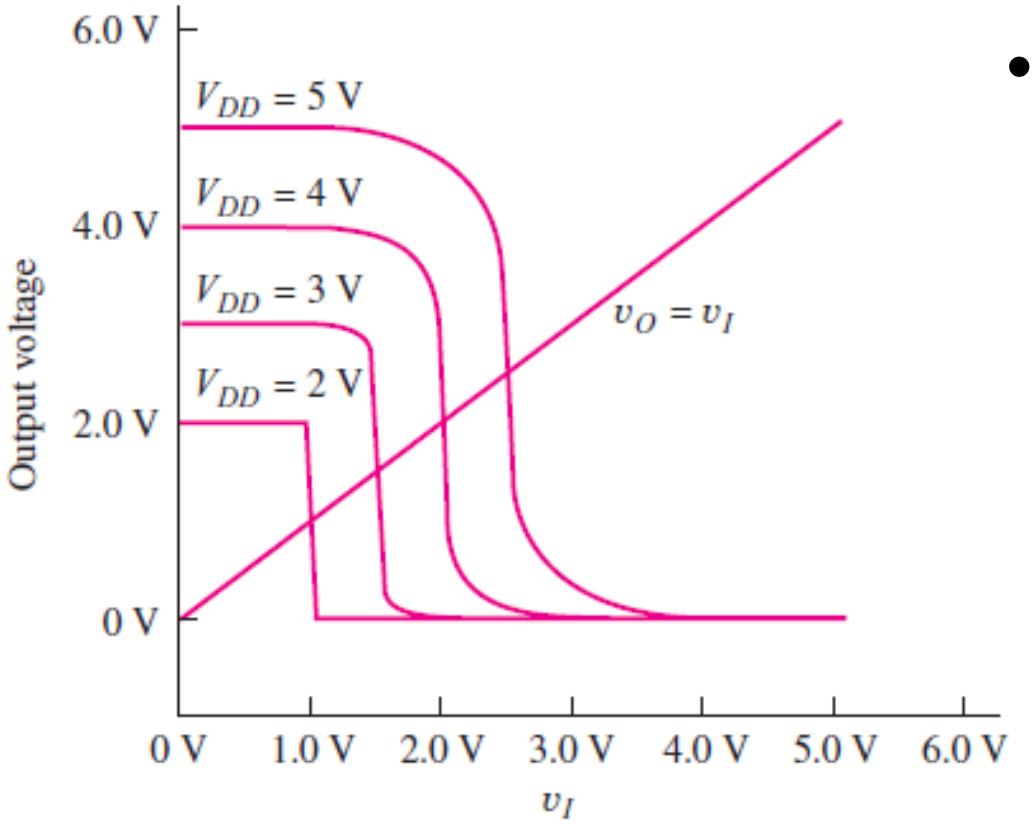
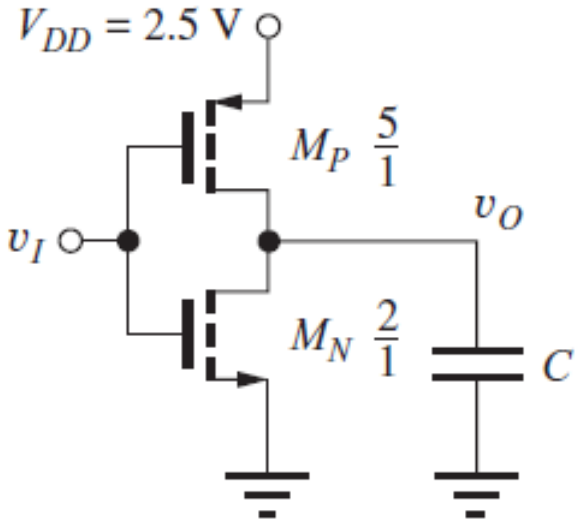
VTC of symmetrical CMOS inverter



$$\mu_n = 2.5\mu_p \Rightarrow \left(\frac{W}{L}\right)_p = 2.5\left(\frac{W}{L}\right)_n$$

- If $K_n = K_p$, transition between V_H and V_L centered at $V_I = V_{DD}/2$



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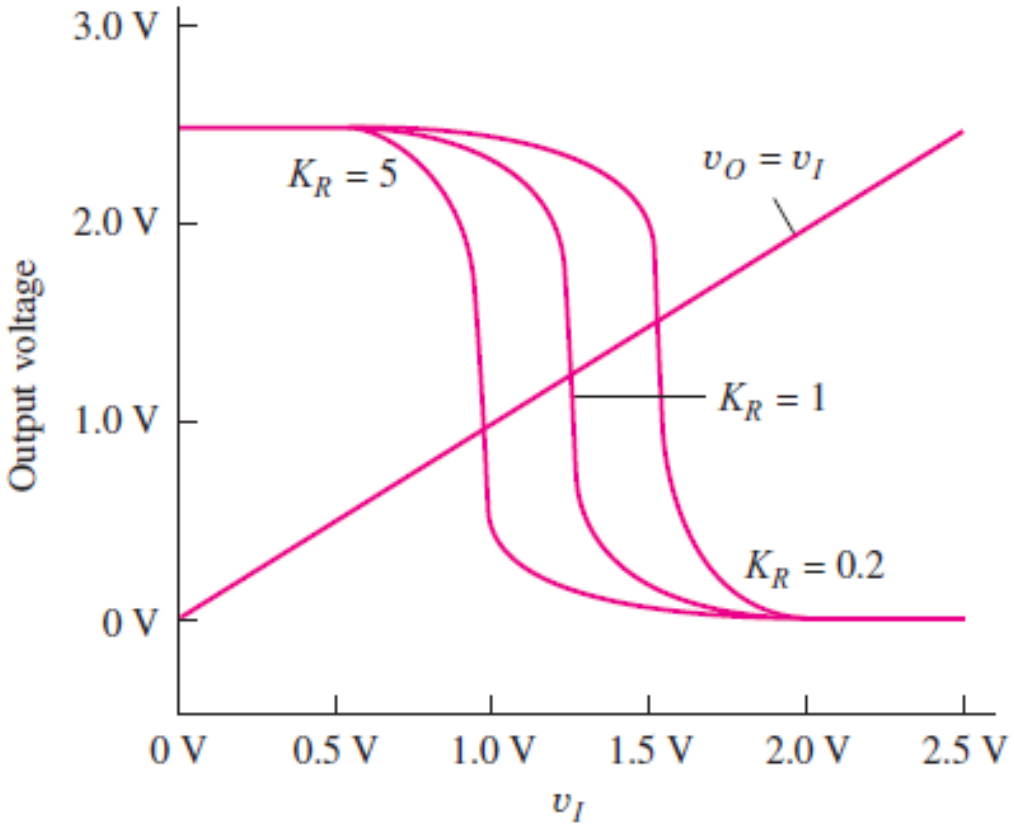
VTC of asymmetrical CMOS inverter



- If $K_n \neq K_p$, transition between V_H and V_L shifts from $V_{DD}/2$
- Define $K_R = K_n / K_p$
- $K_R > 1$, transition shifts to left
- $K_R < 1$, transition shifts to right

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